In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**

In the Claims:

Claims 1-19 (Cancelled).

20. (Currently Amended) A method of transmitting data between a master device and a slave device ~~two devices~~ via a clock line and at least one data line, the clock line being maintained by default on a first logic value, the method comprising:

providing each master and slave device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

tying the clock line to the second logic value, via the ~~two~~ master and slave devices, after data is applied to the data line;

maintaining the tie to the clock line by ~~the device~~ a first device of the master and slave devices to which the data is sent while the first device has not read the data; ~~and~~

maintaining the data on the data line by ~~the device~~ a second device of the master and slave devices sending the data at least until an instant when the clock line is released by the second device to which the data is sent; and

wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device, and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value

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and reads the data, when the slave device is receiving the data from the master device; and

wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device, and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

Claims 21-23 (Cancelled).

24. (Currently Amended) A method according to Claim 20 ~~Claim 23~~, wherein a time.period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

Claims 25-27 (Cancelled).

28. (Currently Amended) A method according to Claim 20 ~~Claim 21~~, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

Claims 29-30 (Cancelled).

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31. (Previously Presented) A method according to Claim 20, wherein the first logic value is 1 and the second logic value is 0.

32. (Currently Amended) A method of transmitting data between a master device and a slave device ~~two devices~~ connected via a clock line and at least one data line, the method comprising:

maintaining the clock line on a first logic value as a default;

providing each master and slave device with the ability to tie the clock line to a potential representing a second logic value;

tying the clock line to the second logic value, via the ~~two~~ master and slave devices, after data is applied to the data line;

maintaining the tie to the clock line by ~~the device~~ a first device of the master and slave devices to which the data is sent while the first device has not read the data; ~~and~~

maintaining the data on the data line by ~~the device~~ a second device of the master and slave devices sending the data at least until the clock line is released by the second device to which the data is sent; and

wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device, and

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wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device; and

wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device, and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

Claims 33-35 (Cancelled).

36. (Currently Amended) A method according to ~~Claim 35~~ Claim 33, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

Claims 37-39 (Cancelled).

40. (Currently Amended) A method according to ~~Claim 33~~ Claim 32, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

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Claims 41-42 (Cancelled).

43. (Previously Presented) A method according to Claim 32, wherein the first logic value is 1 and the second logic value is 0.

Claims 44-47 (Cancelled).

48. (Currently Amended) A synchronous data transmission system comprising:

a clock line;

a data line;

a master data transmitting/receiving device comprising

a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value, and

a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the

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first logic value, when the data is to be sent; and

a slave data transmitting/receiving device comprising

a clock line connection terminal connected to the clock ~~line;~~ line,

at least one data line connection terminal connected to the data ~~line;~~ line,

a circuit for tying the clock line to the potential representing the second logic value, ~~value;~~ ~~and~~

a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received; and

wherein said master device ties the clock line to the second logic value after applying data to the data line when said master device is sending the data to said slave device, and wherein said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from said master device; and

wherein said master device ties the clock line to the second logic value when said master device receives data from said slave device, and wherein said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when said slave device is sending data to said master device.

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49. (Currently Amended) A system according to Claim 48, wherein said ~~the~~ master device further comprises a data receiving unit for waiting for the clock line to have the first logic value~~, tying the clock line to the second logic value, reading the data on the data line, then releasing the clock line, when the data is to be received by the master device~~.

50. (Currently Amended) A system according to Claim 48, wherein said ~~the~~ slave device further comprises a detector for detecting a change from the first logic value to the second logic value on the clock line~~, tying the clock line the second logic value, applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device~~.

Claims 51-52 (Cancelled).

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